RESPONSE A **July 12, 2005**
SER. NO. 09/996,342
ATTORNEY DOCKET NO.: WASC1821

* * * R*E*M*A*R*K*S * * *

Applicants herewith submit this Response in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicants respectfully request this Amendment be entered and further request re-examination and reconsideration of the above referenced patent application in view of the remarks as set forth below. If allowance of the Claims is not forthcoming as a consequence of this response, then the response should be entered in any case, as it puts the application in better condition for consideration on appeal.

Rejections under 35 U.S.C. §102

The Examiner has rejected Claims 1-16 under 35 U.S.C. § 102(a) as being anticipated by Waschura, et al., (European Patent Application EP 1 143 654). The Applicants respectfully traverse the rejection of the aforementioned claims for the reasons set forth in greater detail below.

In rejecting the claims as being anticipated (under 35 U.S.C. §102(a)) by Waschura, the Examiner states on page 13 of the instant Office Action that:

> "...The examiner reminds to the applicants that during patent examination, the pending must be "given the broadest reasonable interpretation consistent with the specification..." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified..."

However, for a claim to be properly anticipated under 35 U.S.C. §102(a), "...each and every element as set forth in the claim [must be] found, either expressly or inherently described, in a single prior art reference..." MPEP 2131. In the instant Office Action, the examiner has not provided such one-to-one correspondence as at least one limitation in each claim is not disclosed by Waschura, et al. In reviewing the Office Action, and the underlying reasons for rejecting the claims, the Examiner either

misunderstood the claimed invention, or misinterpreted the cited reference. But in either event, each and every element of the aforementioned claims is not disclosed in Waschura, et al. Consequently, Waschura, et al. does not anticipate the claimed invention.

Claims 1-6

In rejecting Claim 1, the Examiner states, for example, on pages 2-3 of the instant Office Action that:

> "...Thomas Eugene, James Roger, Robert Lee disclose apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator (abstract, fig. 2, unit 203, 200), and logic means for accumulating time and voltage event counts (Col. 4-6, section 0017-0019) of the bit stream pulses falling within voltage threshold and points inside the window comparator during durations of the binary bit stream and drawing eye diagrams therefrom defining the bit stream characteristics..."

Thus, as understood from the above presentation of elements, the Examiner is asserting that the count logic of Waschura, et al. is the same as the "...window comparator..." limitation of Claim 1. Such assertion is contrary to the disclosure of Waschura, et al., which must be considered when rejecting the pending claims. MPEP2131. As such, Waschura, et al. does not anticipate each and every limitation of Claim 1.

For example, Claim 1 is directed to an apparatus for measuring characteristics of a bit stream of binary pulses, which includes the following limitations:

> "...control means for defining a window comparator..." and
>
> "...logic means for accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during durations of the binary pulse bit stream..."

Waschura, et al. is silent on the above; therefore, Waschura, et al. does not disclose each and every limitation of the claimed invention. Consequently, Waschura, et al.

does not anticipate the invention as defined in Claim 1. As understood, and as illustrated, for example, in FIG. 2 and as described, for example, in the Abstract, on paragraph 16, lines 1-4; paragraph 17, lines 1-11; paragraph 19, lines 1-3 and lines 5-7, Waschura, et al. is directed to a "...measuring apparatus for sampling pulse voltage levels in excess of a voltage threshold levels during each of delayed clock pulses..." Although the threshold voltage level may vary during in a different time period (paragraph 17, lines 3-7), such voltage levels act as the individual threshold values of interest- not a window of values as defined in Claim 1.

As illustrated, for example, in FIG. 2 and as described, for example, paragraph 19, lines 1-3:

> "...Count logic 20 has a one-bit comparator 200 with one input connected to the transmission facility 12 or other point in the transmitter 10 or receiver 11 to measure the high speed binary coded bit stream...."

And as further disclosed in paragraph 19, lines 5-7:

> "...The one-bit comparator 200 will output a high when the signal voltage on the positive pin is higher than the signal voltage on the negative pin..."

Thus, Waschura, et al. discloses a single threshold value element that outputs a logical one when the input signal voltage is greater than the threshold value. The single (e.g. threshold) value cannot and does not behave as a window or two value element as the disclosure appears to be silent on such an element. In contrast, the "...window comparator..." of Claim 1 is illustrated in Fig. 2 and described, for example, in paragraph 20, lines 11-15 as being a control apparatus that:

> "...applies a value of voltage V + ΔV 200 to the plus input of comparator 202 and a value of voltage V, 201, to the minus input of comparator 203 to create a voltage threshold window..."

Thus, the window as defined in Claim 1 is defined as being bounded by two values: an upper voltage value of V + ΔV; and a lower voltage value of V. Thus, the claimed window comparator of the instant invention defines a voltage window area defined by

upper and lower voltage values. The single value comparator (e.g. comparator 200) of Waschura, et al. does not correspond to the window comparator of Claim 1.

In corresponding fashion, the count logic (e.g. about threshold counter 203) of Waschura, et al. does not correspond to the count logic of Claim 1 in that the count logic of Waschura, et al does not:

> "...accumulating time and voltage counts of the bit stream pulses falling within voltage thresholds and points inside the window comparator during durations of the binary pulse bit stream..."

as the circuit described in Waschura, et al. is not cable of defining a voltage window; thus, it is not capable of counting instances of a voltage being within voltage thresholds. The circuit of Waschura, et al. determines and counts when an input voltage signal exceeds a lower limit threshold value. Thus, this limitation of Claim 1 is not disclosed by Waschura, et al. Consequently, as neither of the aforementioned limitations of Claim 1 is disclosed in Waschura, et al. the Applicants respectfully submit that Waschura, et al. does not anticipate the invention as defined in Claim 1. Accordingly, reconsideration of the rejection of Claim 1 is respectfully requested.

Claims 2-6 directly or indirectly depend upon and include the limitations of Claim 1 and are submitted to be allowable at least for the reasons set forth above with respect to Claim 1. In additions, these claims define subject matter that is independently allowable over the art of record. More specifically, Claims 2-3 are directed to the method employed by the control means for creating the voltage threshold window, and the detecting of voltage levels within the boundaries of the voltage threshold window, respectively. As discussed in greater detail above, Waschura, et al. is silent on the use or creation of a threshold window or a window comparator or the detection of voltage values that fall within a given threshold window. Thus, Waschura, et al. also does not anticipate at least Claims 2-3. Accordingly, reconsideration of the rejection of Claims 1-6 is respectfully requested.

Claim 7

Claim 7 is directed to an apparatus for measuring characteristics of a bit stream of binary pulses that includes a limitation directed to "...control means for defining a window comparator..." As discussed in greater detail above, with respect to Claim 1, Waschura, et al. is silent on generating a window comparator as Waschura, et al. is directed to determining and counting when an input signal voltage exceeds a single threshold value; not determining and counting when an input signal voltage is within a voltage window. Thus, at least this limitation of Claim 7 is not disclosed in Waschura, et al.

Additionally, Claim 7 further defines the measuring apparatus as including an "...apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels...and for accumulating counts...when the pulse voltage levels are within the voltage threshold window..." Thus, Claim 7 clearly defines the generation of a threshold window bounded by "...minimum and a maximum voltage levels..." Waschura, et al. does not disclose such a structure as Waschura, et al. discloses for example, in FIG. 2 and paragraph 19, lines 1-7 a single threshold value comparison circuit. Consequently, as Waschura, et al. does not disclose a component that generates a threshold window bounded by "...minimum and a maximum voltage levels..." Waschura, et al. does not disclose each and every limitation recited in Claim 7. Therefore, Waschura, et al. does not anticipate the invention as defined in Claim 7. Accordingly, reconsideration of the rejection of Claim 7 is respectfully requested.

Claim 8

Claim 8 is directed to an apparatus for measuring characteristics of a bit stream of binary pulses. Claim 8, like Claim 7 above, includes limitations directed to:

> "...control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold..." and
>
> "...means for detecting...when the pulse voltage levels are within the voltage threshold..." window

As such, Claim 8 is submitted to be allowable at least for the reasons set forth above with respect to Claim 7. Accordingly, reconsideration of the rejection of Claim 8 is respectfully requested.

Claims 9-14

Claim 9 is directed to a method for determining the characteristics of a bit stream of binary pulses, including the following limitations:

> "...defining a window comparator..." and
>
> "...accumulating voltage threshold counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream within voltage thresholds at points inside the window comparator ..."

Thus, Claim 9 recites a method where a window comparator is defined, and then counting the number of pulses having voltage values that fall within (or inside) the window comparator. As discussed in greater detail above, the window comparator of the instant invention is an area bounded by an upper voltage limit (V+ΔV) and a lower voltage limit (V). See, for example, ¶ 20, lines 1-5 and 11-15. Waschura, et al. does not disclose the aforementioned steps as it is silent on the use of a voltage window; instead, Waschura, et al. detects and counts the number of times an input signal voltage exceeds a single threshold value (See, for example, paragraph 19, lines 1-7). Thus, Waschura, et al. does not disclose the aforementioned limitations of Claim 9. Accordingly, reconsideration of the rejection of Claim 9 is respectfully requested.

Claims 10-14 directly or indirectly include the limitations of Claim 9 and are allowable at least for the reasons set forth above with respect to Claim 9. In addition, these claims defines subject that is independently allowable over the art of record. More specifically, Claims 11-12 include limitations directed to:

> "...creating a voltage threshold window that moves with respect to a minimum and maximum voltage threshold..." and

> "...detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window..."

As discussed in greater detail above, Waschura, et al. discloses a signal characteristic determination method that counts the number of times an input voltage signal exceeds a single threshold value. Waschura, et al. is silent on the use of a bounded voltage threshold window or counting the number of times an input voltage signal level falls within the bounded window. Thus, Waschura, et al. does not disclose each and every limitation of the claimed invention. Accordingly, reconsideration of the rejection of Claims 9-14 is respectfully requested.

Claim 15

Claim 15 is directed to a method for determining characteristics of a bit stream of binary pulses, such as would be performed, for example, by the apparatus defined in Claim 7. Claim 15, like Claim 7 above, includes limitations directed to:

> "...creating a voltage threshold window that moves between a minimum voltage and a maximum voltage..." and
>
> "...accumulating counts of voltage levels of the binary pulses...within the voltage threshold window..."

As such, Claim 15 is submitted to be allowable at least for the reasons set forth above with respect to Claim 7. Accordingly, reconsideration of the rejection of Claim 15 is respectfully requested.

Claim 16

Claim 17 is directed to a method for determining characteristics of a bit stream of binary pulses, such as would be performed, for example, by the apparatus defined in Claim 8. Claim 16, like Claim 8 above, includes limitations directed to:

> "...creating a voltage threshold window that moves between defined voltage levels..." and

"...detecting voltage levels of binary pulses...within the voltage threshold window..."

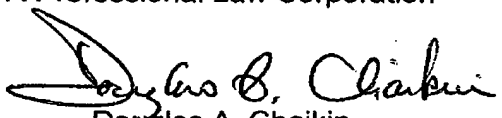
As such, Claim 16 is submitted to be allowable at least for the reasons set forth above with respect to Claim 7. Accordingly, reconsideration of the rejection of claim 15 is respectfully requested.

CONCLUSION

Having answered each and every ground of rejection as set forth by the Examiner, the Applicants respectfully submit that Claims 1-16 are now in proper condition for allowance and such action is earnestly solicited. The Applicants now request that this Response be considered and that it be entered on the record. The Examiner is invited to contact the undersigned if such action might expedite the prosecution of the above-noted application or if the Examiner feels that there are pending issues that need to be resolved.

Respectfully submitted

PENINSULA IP GROUP
A Professional Law Corporation



Douglas A. Chaikin
26150 Bucks Run
Corral de Tierra, CA 93908
Telephone: (831) 484-2641
(Fax): (831) 886-2488
Reg. No.: 29,140